



Memory

Beyond Barriers: Enabling Future AI

PERSISTENT RERAM FROM 4DS MEMORY

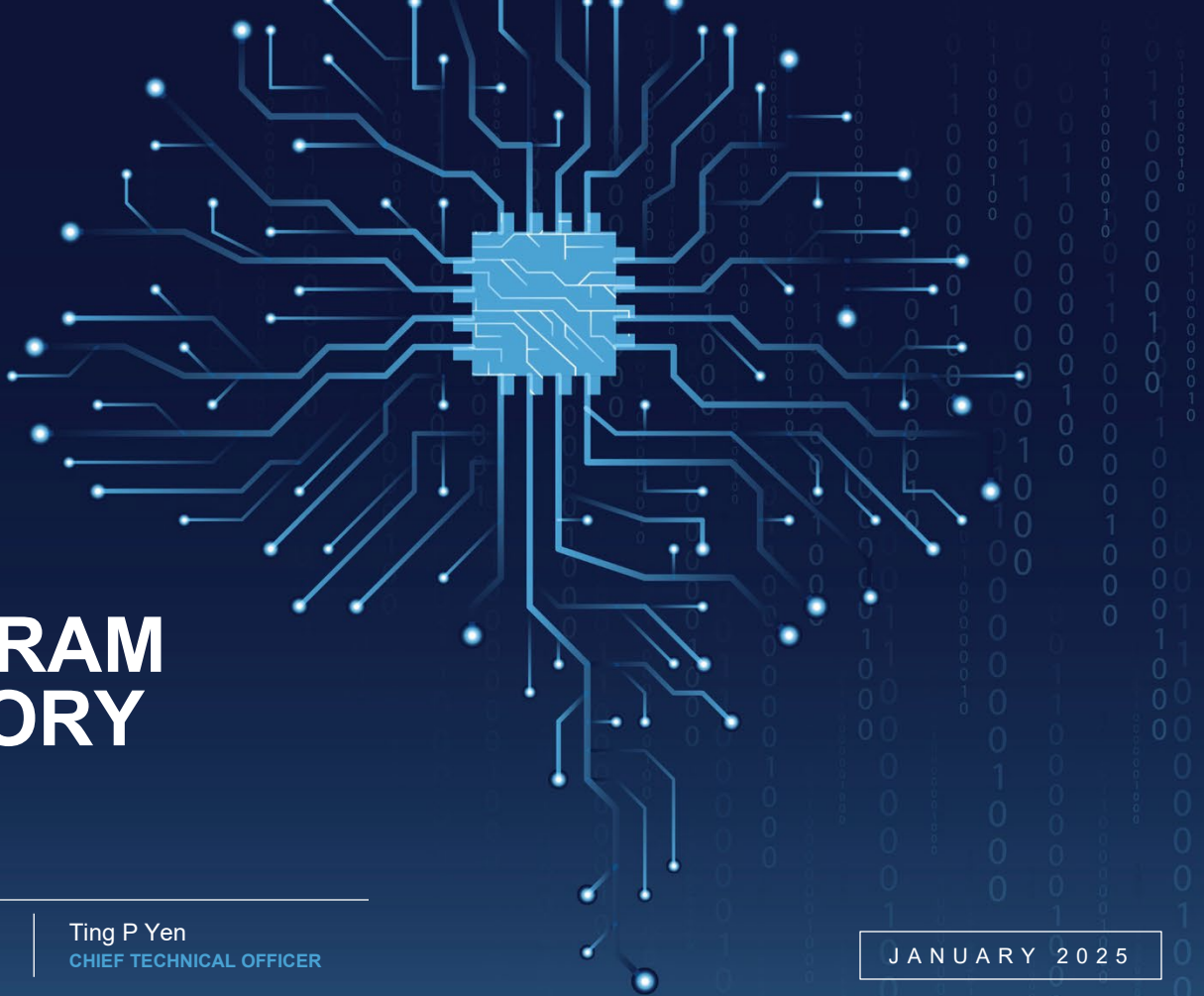
CAPITAL RAISE

David McAuliffe
EXECUTIVE CHAIRMAN

Peter Himes
CHIEF STRATEGIC OFFICER

Ting P Yen
CHIEF TECHNICAL OFFICER

JANUARY 2025



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4DS: The Right Memory for the Right Market at the Right Time



4DS Overview	<ul style="list-style-type: none">• Based in Silicon Valley, 4DS is developing a high speed, high endurance and low energy memory technology to enable future AI systems.• 4DS' unique PCMO ReRAM technology will bridge the gap between volatile DRAM (fast & short term) and non-volatile FLASH memory (slow & long term), offering an important solution to known limitations of warm data, big data and AI applications.
Demonstrated Technology	<ul style="list-style-type: none">• Through its strategic relationship with imec, 4DS is the only company to demonstrate PCMO ReRAM on an advanced CMOS node.• imec is the worlds largest independent research and innovation centre, specialising in nanoelectronics and digital technologies, with over 5,500 scientists and engineers headquartered in Belgium.• 4DS has demonstrated extremely fast single-shot write times (DRAM speeds) at low energy per bit whilst retaining high bandwidth and high endurance.
Solving future AI challenges	<ul style="list-style-type: none">• In current AI computing, data transfer between processing units (logic) and memory/storage consumes up to 200 times the energy used in computation• Fast and efficient non-volatile memory solutions like 4DS' PCMO ReRAM are the key to unlock in-memory and near memory computing.• Global memory technology market forecast to be > US\$200B by 2030
Commercial Strategy	<ul style="list-style-type: none">• 4DS has established high value engagements with imec, Infineon Technologies and a top 2 Taiwanese foundry• The agreement with Infineon Technologies (Market Cap A\$71 billion) will leverage their deep expertise in designing and developing memory chips and 4DS' expertise in PCMO ReRAM• Following successful development of the memory test chip by Infineon 4DS will be well placed to explore commercial M&A and partnering opportunities
Key Catalysts	<ul style="list-style-type: none">• Key upcoming catalysts for 4DS include:<ul style="list-style-type: none">○ Completion of testing and characterisation of Fifth Platform Lot – process tuning for 20nm node – Announced 15 January 2025○ Commencement of Infineon development agreement – Q1 2025○ Results of Sixth Platform Lot – Demonstration of working 4DS memory at 20nm node – 1H 2025
Capital Raising	<ul style="list-style-type: none">• 4DS is seeking to raise up to approximately \$8m via a \$6m Placement and \$2m SPP. Funds will be used for payments to Infineon, ongoing investment in development with imec, general working capital and offer costs.

World Class Management Team



Mr Ting P Yen
Chief Technology Officer

- Over 30 years of semiconductor experience
- Expert in semiconductor memory architecture / process integration
- Long career in the heart of Silicon Valley with semiconductor pioneers: Fairchild, Hewlett Packard and Philips Research
- Managed the Advanced Memory program at Cypress Semiconductor (subsequently acquired by Infineon)
- Held key engineering management roles in advanced Research & Development of memory platforms including SRAM, Ternary CAM, Non-Volatile Flash memory and Emerging memory
- 21 US Patents and a Master's of Science Chemical Engineering from the University of California, Santa Barbara.



Mr David McAuliffe
Executive Chairman

- Experienced board director and entrepreneur who has over 24 years' corporate experience and been involved in numerous capital raisings and in-licensing of technologies
- Founder of several companies in Australia, France and the United Kingdom, many of which have become public companies
- Bachelor of Laws (Honours), a Bachelor of Pharmacy, is Interim Non-Executive Chairman of Invex Therapeutics Ltd and is the President of the Dyslexia-Speld Foundation WA (Inc).



Mr Peter Himes
Chief Strategic Officer

- Over 35 years in high growth technology firms, with extensive general management, sales and business development responsibilities
- Skilled at building winning teams, defining and addressing new markets, building key relationships and partnerships across the value chain, and promoting and evangelizing for business opportunities
- Consistently recognized as a thought leader across multiple industries with a strong focus on innovation systems and strategic alliances



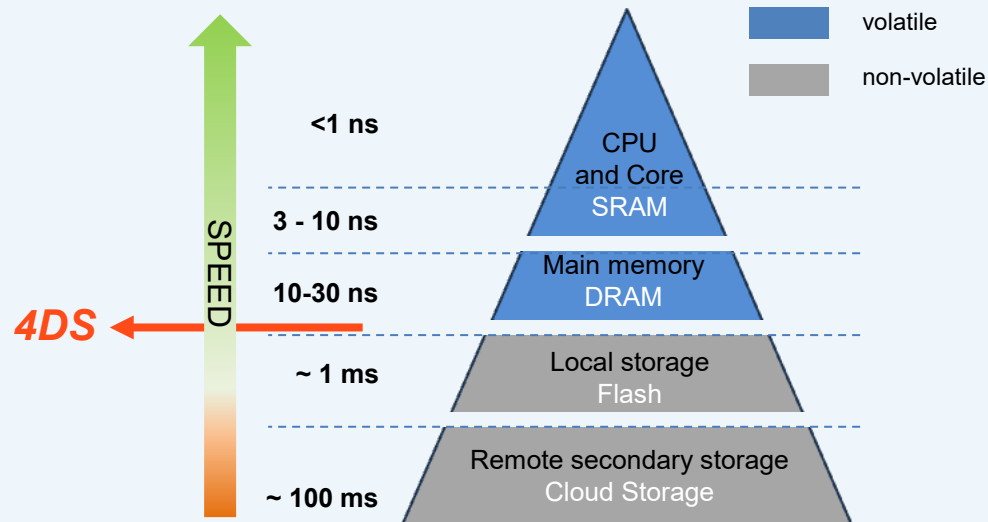
4DS Fits Uniquely Into The Existing Memory Hierarchy

System memory architectures generally trade off between speed and capacity

To date there is a gap between the high speed (but volatile) DRAM and the high density (but slow) Flash

4DS Memory is uniquely positioned to fill this gap

- **As fast as DRAM**
- **Persistent retention**
- **High endurance**
- **Gigabit scale achievable**



4DS Technology

The technology behind **4DS Memory** is a type of **Persistent Resistive Random Access Memory (ReRAM)** which switches the memory cell between a '1' or '0' state, in the digital sense.

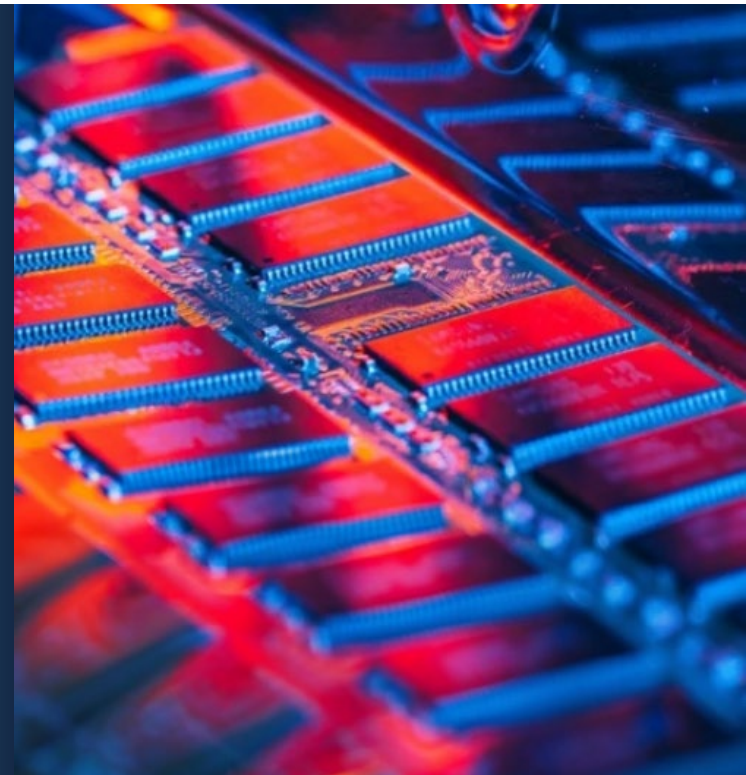
The 4DS cell is based on a different physical switching mechanism called **Area Based Interface Switching**.

Most other ReRAM on the market is called filamentary which holds various performance limitations.

Our switching mechanism gives us the high speed, high endurance and tunable retention characteristics that position 4DS uniquely in the market and potentially fulfilling the limitations imposed on filamentary ReRAM.

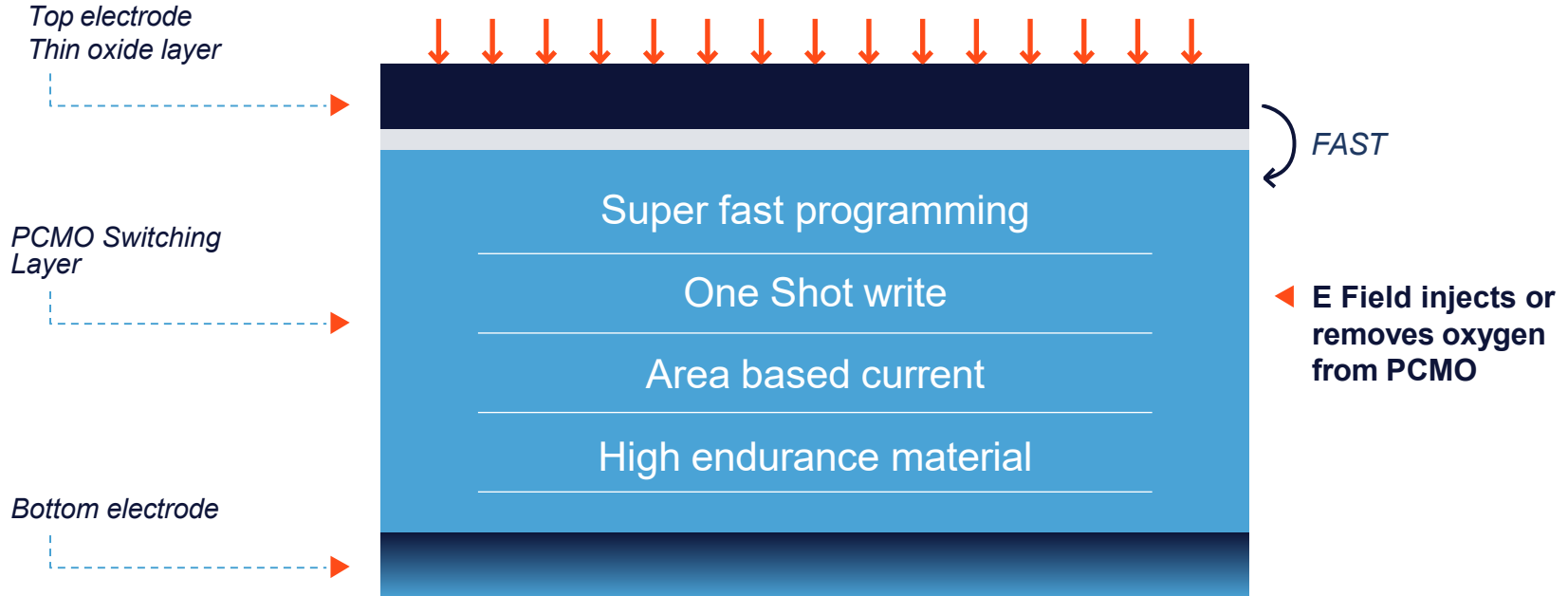
Memory can be broadly divided into Volatile and Non-Volatile (NV) technologies

- Volatile memories (DRAM or SRAM) deliver high speed and endurance but require constant power to be usable.
- Non-Volatile (NV) technologies retain their data without power or refresh, but at slow write speeds and limited endurance.



Area Based Interface Switching

Current is spread across entire interface area.
Low current densities lead to high cell endurance.



The 4DS Advantages



Persistent Memory at DRAM Speeds

Single write pulse for hours to days of retention

DRAM speeds means no system performance compromises

Tunable Retention from Hours to Days

Highest energy optimization for warm data applications

Can trade off endurance for longer retention when required

Low Energy per Bit

For Warm Data and Persistent Memory Applications

Scalable to Any Process Node

Simple fab processing, compatible with modern fabs

Low-cost BEOL Integration, compatible to any advanced CMOS process nodes

Analog Programmability

By time or voltage modulation

Importance of 4DS for Today's Applications



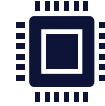
Persistent Memory for Big Data

Combines DRAM speed with adequate data retention for faster data access and improved system reboot. Integrates seamlessly into the memory hierarchy, residing between memory and storage devices



Warm Data Applications

Operates at DRAM speeds without constant updating, lowering energy costs in AI inference and enhancing memory efficiency. In Memory or Near Memory Compute compatible.



Edge AI Applications

Meets high performance in resource-constrained, battery powered devices with low energy consumption and efficiency focus

4DS Commercialisation Pathway

Significant technical de-risking achieved. Material technical and commercial milestones over the coming 18 months



4th Platform Lot: Groundbreaking Results

4TH PLATFORM LOT

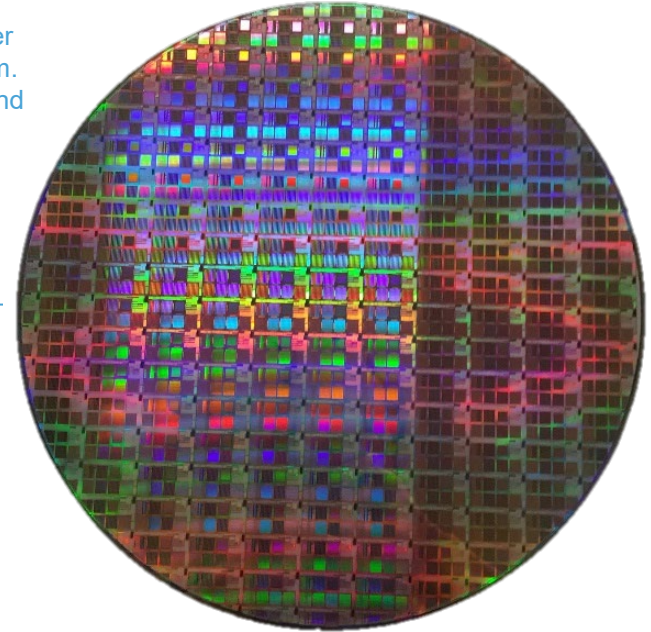
PURPOSE

Demonstrate Megabit Array Performance of 4DS Memory

RESULTS

- ✓ Demonstrated write speed at DRAM speed
- ✓ Persistent memory with variable and tuneable retention
- ✓ Analog programming capability
- ✓ Single shot pulse programming
- ✓ Low energy consumption

Picture of 4DS wafer out of imec, Belgium. This wafer image and circuit design are copyright imec and are used with permission.



imec Development – Update



5TH PLATFORM LOT

PURPOSE

Tune and verify necessary process adjustments on the 60nm cell to support 20nm cell (Lot 6) manufacturing.

STATUS

- ✓ Successfully manufactured by imec on 10 October 2024 and shipped to 4DS facilities in California
- ✓ Majority of testing completed. New process refinements applied to processing of the 20nm cell manufacturing (in progress)
- ✓ Completion of testing and characterization

6TH PLATFORM LOT

PURPOSE

To demonstrate scalability of 4DS technology to 20nm node (Gigabit density compatible)

EXPECTED OUTCOMES /

DATA POINTS:

- Demonstrate working 4DS memory at 20nm node
- Confirmation of a scalable technology which is critical for any potential licensee or acquirer

STATUS

- Completion of manufacturing by imec and testing completed expected 1H 2025

FUTURE IMEC/4DS DEVELOPMENT

PURPOSE

Optimisation of 4DS PCMO ReRAM in support of Infineon design and development

STATUS

- Ongoing

WHO IS IMEC?

- imec is the worlds largest independent research and innovation centre specialising in nanoelectronics and digital technologies
- Cutting-edge facilities, including a 4-billion-euro semiconductor pilot line
- FY22 Revenue of €850m
- Over 5,500 scientists and engineers headquartered in Belgium

Infineon Technologies Design Agreement

- 4DS will work with imec, Infineon Technologies LLC (Infineon) and a first Tier Taiwanese foundry to design and build a custom ReRAM Test Chip

- This Test Chip will be based on the unique requirements of the 4DS Interface Switching ReRAM Technology

- The Infineon Technologies Design Agreement (Agreement) leverages Infineon's deep expertise in designing and developing memory chips and 4DS' expertise in PCMO ReRAM

- The Agreement covers a 15-month project timeline at a cost to 4DS of USD\$4.5M with an up front payment of USD\$1.5M, followed by a schedule of monthly payments

- The deliverable of the Agreement is a fully designed and verified Memory Test Chip which will accelerate discussions with potential commercial partners and acquirers



Infineon Technologies AG is Germany's largest semiconductor manufacturer. As a global semiconductor leader Infineon Technologies AG has:

- Listings on the Frankfurt Exchange and the USA OTCQX
- A market capitalisation of more than €40 billion
- Revenue in fiscal year 2023: more than €16 billion
- About 58,600 employees worldwide (as of September 2023)
- 69 R&D locations; 17 manufacturing locations

Source: Google Search

Value Chain for Memory Test Chip Development

	CUSTOM TEST CHIP	4DS Memory	infineon	umec	1st Tier Foundry
DESIGN	• Architecture/ Definition ↓	✓	✓		
	• Design / Verification ↓	✓	✓		
	• Design TAPEOUT ↓	✓	✓	✓	
FABRICATION	• Front End Fabrication ↓				✓
	• Back End Fabrication ↓	✓		✓	
	• Fabrication Complete ↓			★	
TEST	• Test Chip Testing	✓			

Significance of the Infineon Agreement

Infineon Agreement:

- The next step in technology development is to develop a Memory Test Chip fully customized to the 4DS technology
- Developing the Memory Test Chip independently would be prohibitively expensive and high risk
- Signing with Infineon aligns 4DS with a world leading team with decades of experience in memory chip design



4DS Strategic Objective: Licensing and/or M&A:

- Commercial engagement requires 4DS to demonstrate clear superiority of its memory technology for emerging applications.
- Development of a Memory Test Chip allows potential partners to test a Memory Chip and benchmark our technology.
- This Test Chip will allow potential partners to validate the unique advantages of 4DS memory in their system architecture

Key Catalysts & Outlook



Announced 15 January 2025



Completion of testing and characterisation of Fifth Platform Lot: Pre 20nm process tuning

Q1 CY25



Commencement of 4DS – Infineon Design Services memory test chip development

Expected 1H 2025



Results of Sixth Platform Lot: First demonstration of 4DS at 20nm node

Expected 1H CY26



Manufacturing & testing of validation lot at imec

Expected 1H CY26



Completion of 4DS Memory Test Chip design, verification and tape out

Expected 2H 2026



Memory Test Chip fabrication and testing

Ongoing Engagement



With potential commercial partners including tier 1 semiconductor manufacturers

Capital Raising Overview

Placement	<ul style="list-style-type: none">• A Placement to sophisticated and professional investors of approximately \$6.0m, comprising;<ul style="list-style-type: none">▪ The issue of approximately 166.7 million new shares in the Company ("New Shares") under the company's existing placement capacity per LR7.1 & 7.1A ("Placement")
Security Purchase Plan	<ul style="list-style-type: none">• 4DS will offer Eligible Securityholders the opportunity to participate in a non-underwritten Security Purchase Plan to raise up to A\$2.0 million ("SPP")• Eligible securityholders in Australia and New Zealand will be invited to subscribe for up to \$30,000 of New Shares free of any brokerage, commission and transaction costs at the same price as the Placement.• 4DS reserves the right to increase the size of the SPP or to scale back applications in its absolute discretion• Further details in relation to the SPP including the timetable will be provided to eligible shareholders in an SPP booklet expected to be released following the Placement
Offer Price	<ul style="list-style-type: none">• New Shares issued under the Placement and SPP will be issued at a price of \$0.036 per New Share ("Offer Price"), representing a:<ul style="list-style-type: none">▪ 12.2% discount to the last close price on 14 January 2025 of \$0.041▪ 24.4% discount to 15 trading day VWAP of \$0.0476
Attaching Options	<ul style="list-style-type: none">• Shares will be offered under the Placement and SPP with one (1) free attaching option for every one (1) New Share issued ("Attaching Options").• The Options will be unlisted with an exercise price of \$0.036 and will expire on 28 February 2028.
Use of Funds	<ul style="list-style-type: none">• Working capital requirements under the design and services agreement with Infineon, ongoing investment in development with imec, general working capital and offer costs
Ranking	<ul style="list-style-type: none">• All New Shares issued under the Offer will rank equally with existing 4DS Shares from the date of issue
Lead Manager	<ul style="list-style-type: none">• Bell Potter Securities Limited ("Bell Potter")

Capital Raising Timetable



INDICATIVE CAPITAL RAISING TIMETABLE ¹	DATE
Trading Halt, Bookbuild Opens	<i>Wednesday, 15 January 2025</i>
Announcement of Capital Raising and Trading Halt Lifted	<i>Friday, 17 January 2025</i>
Record Date for the SPP Offer	<i>Thursday, 16 January 2025</i>
Settlement of Placement	<i>Wednesday, 22 January 2025</i>
Allotment of New Shares under the Placement	<i>Thursday, 23 January 2025</i>
Open of the SPP Offer	<i>Friday, 24 January 2025</i>
Close of the SPP Offer	<i>Friday, 14 February 2025</i>
Announcement of results of the SPP Offer	<i>Thursday, 20 February 2025</i>
Allotment of New Shares under the SPP, SPP Options and Placement Options	<i>Friday, 21 February 2025</i>

¹The timetable is indicative only and subject to change by the Company and Lead Manager, subject to the Corporations Act and other applicable laws.

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- is an eligible investor within the meaning of clause 41 of Schedule 1 of the FMC Act.

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Thank **you** for your time.

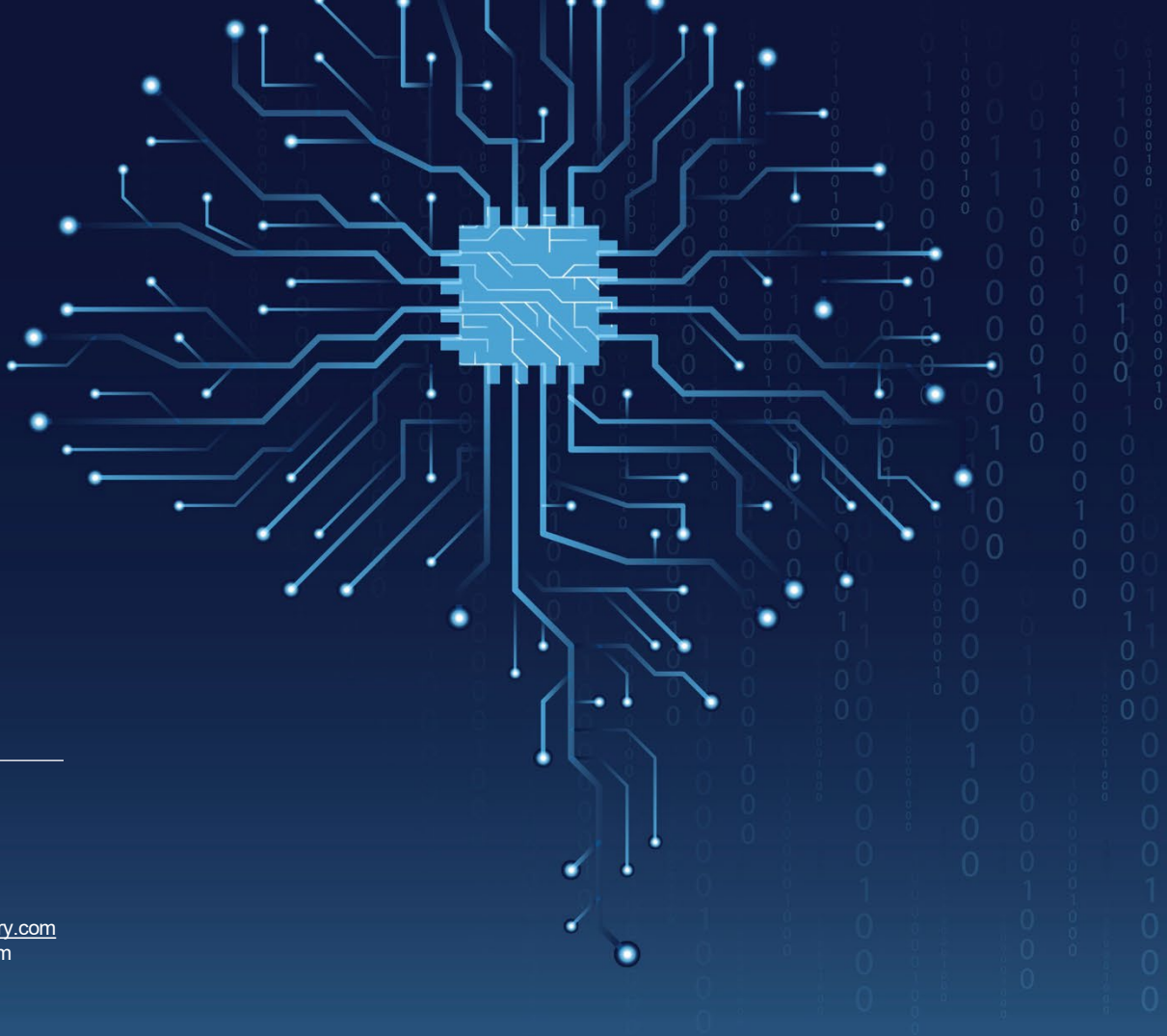


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Memory

Beyond Barriers: Enabling Future AI



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